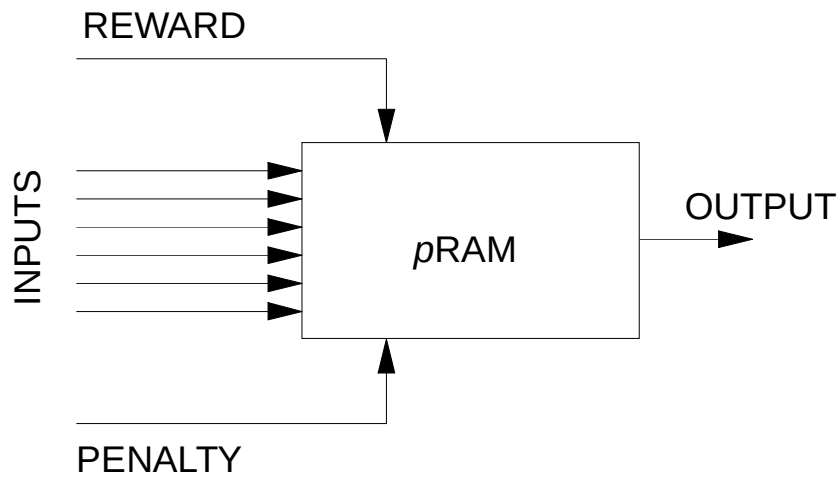
A SINGLE *p*RAM



THERE ARE 256 *p*RAMs IN A *p*RAM-256 MODULE.

THE OUTPUT OF AN INDIVIDUAL *p*RAM IS REPRESENTED BY ONE BIT IN THE SERIAL DATA STREAM FROM **PRAM_OUT**. DATA FROM *p*RAM 0 IS INDICATED BY THE **SOP1** SIGNAL. THE OUTPUTOF A *p*RAM IS ALSO STORED INTERNALLY IN THE *p*RAM-256 SO THAT IT CAN BE APPLIED TO THE INPUTS OF OTHER *p*RAMS INTHE MODULE OR IN NEIGHBOURING MODULES.

*p*RAM MODULES CAN ACCESS *p*RAM DATA IN OTHER *p*RAM MODULES BY SPECIFYING THE MODULE NUMBER IN BITS 8 TO 10 OF AN INPUT CONNECTION POINTER.

USING THE CONNECTION POINTERS ASSIGNED TO EACH INPUT OF EACH *p*RAM, THE CONNECTIVITY OF A NEURAL NETWORK CAN BE SPECIFIED.

CONNECTION POINTERS ALLOW ANY *p*RAM INPUT TO BE CONNECTED TO THE OUTPUT OF ANOTHER *p*RAM (INCLUDING ITSELF), AN EXTERNAL STATE INPUT, A LOGIC '1' OR A LOGIC '0'.

REWARD AND PENALTY INPUTS ARE USED FOR TRAINING THE NEURAL NETWORK. THESE CAN BE CONNECTED TO OTHER DATA SOURCES AS ABOVE. THEY CAN ALSO BE CONNECTED TO A GLOBAL REWARD AND A GLOBAL PENALTY SIGNAL RESPECTIVELY.

USING THE CONNECTION POINTERS, A RANGE OF NEURAL NETWORKS CAN BE BUILT FROM A *p*RAM-256 MODULE AND A RANGE OF TRAINING SCHEMES CAN BE IMPLEMENTED.

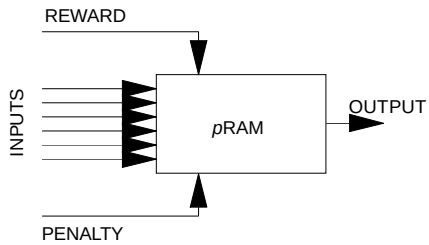
NON-LEARNING *p*RAMS

ANY *p*RAM WITHIN A MODULE MAY BECONFIGURED AS A NON-LEARNING *p*RAM, IRRESPECTIVE OF THE STATE OF THE **TRAIN** INPUT.
THIS IS ACHIEVED BY SETTING THE CONNECTION POINTERS FOR ITS REWARD AND PENALTY INPUTS TO 'GND'. IN THIS WAY, NO MODIFICATION OF THE WEIGHTS IN THAT *p*RAM WILL OCCUR.

FIXED-INPUT *p*RAMS

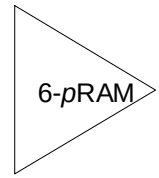
ONE WEIGHT WITHIN THE *p*RAM MAY BE CONTINUOUSLY ACCESSED BY SETTING THE CONNECTION POINTERS FOR ITS INPUTS TO A VALUE OF 'VCC' OR 'GND' AS DESIRED.

NETWORK ARCHITECTURES



FOR CLARITY, THE *p*RAM WILL BE DRAWN AS THE SYMBOL SHOWN.

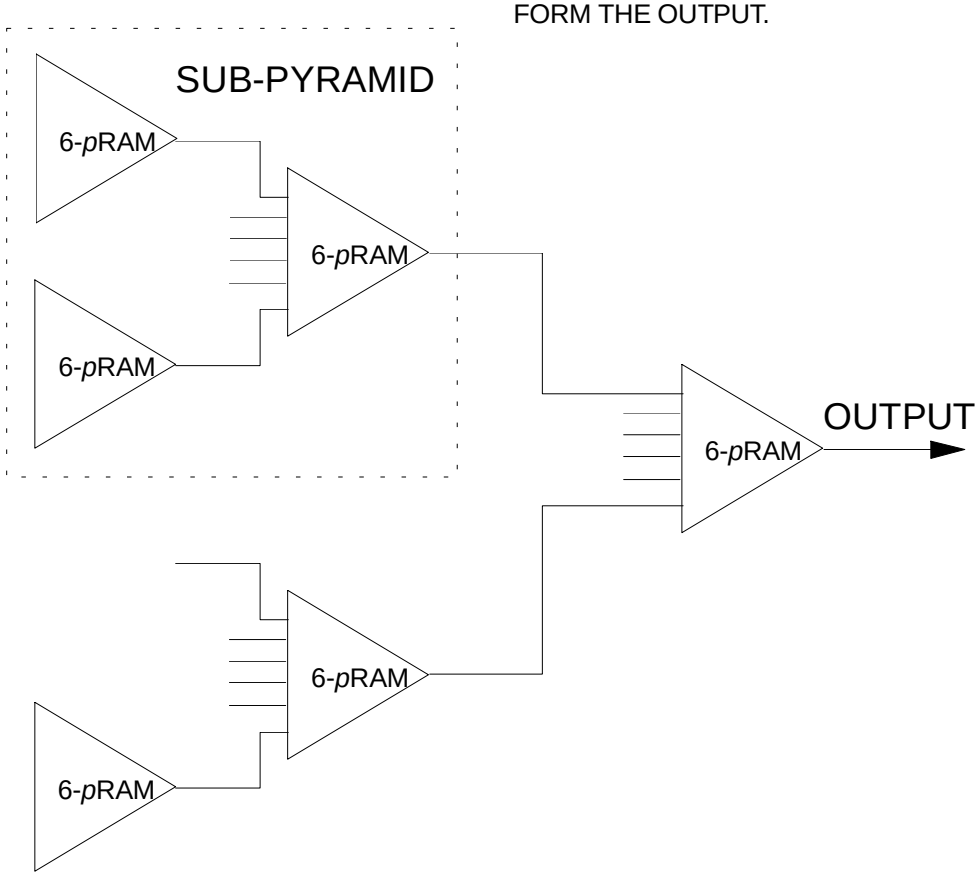
THE REWARD AND PENALTY INPUTS WILL NOT BE SHOWN.



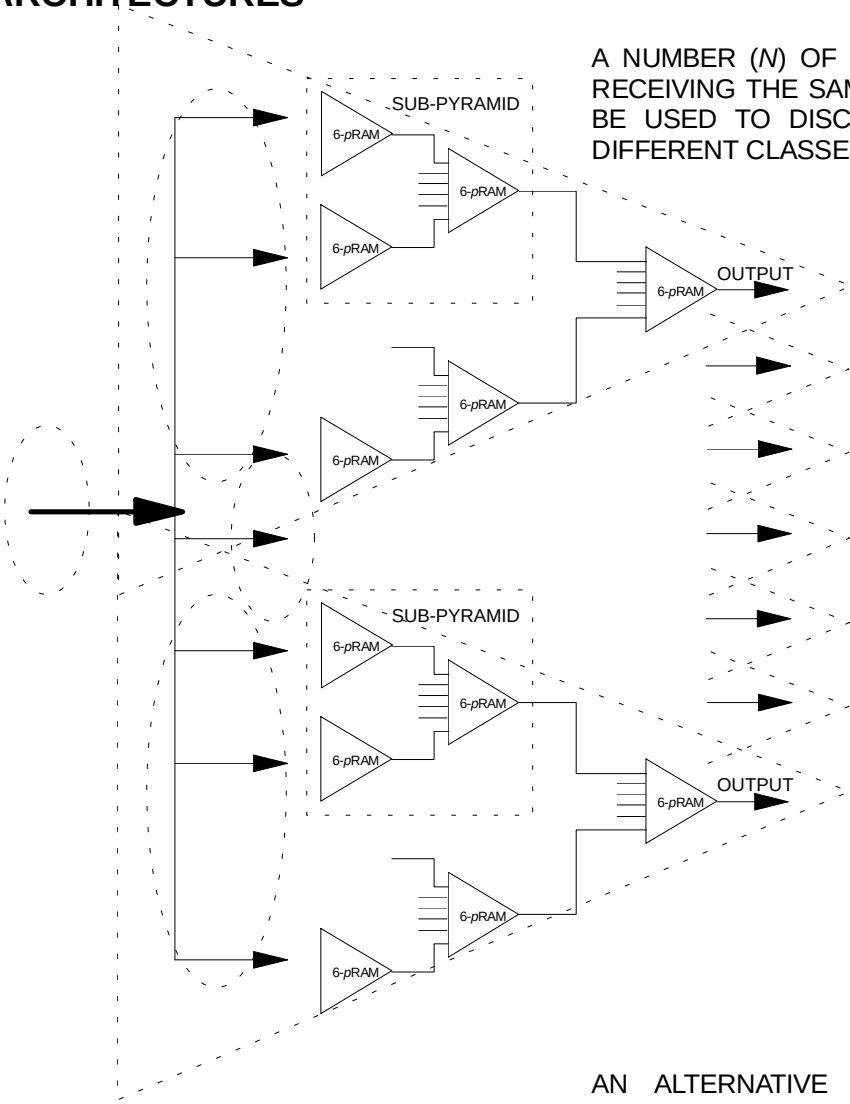
PYRAMIDAL ARCHITECTURES

AS MANY SUB-PYRAMIDS AS ARE REQUIRED ARE BUILT TO RECEIVE THE INPUT VECTOR. AT LEAST N/6 *p*RAMS ARE REQUIRED FOR AN N-INPUT VECTOR.

SUB-PYRAMIDS ARE THEMSELVES COMBINED TO FORM THE OUTPUT.



PYRAMIDAL ARCHITECTURES



A NUMBER (*N*) OF FULL PYRAMIDS, EACH RECEIVING THE SAME INPUT VECTOR CAN BE USED TO DISCRIMINATE BETWEEN *N* DIFFERENT CLASSES OF INPUT.

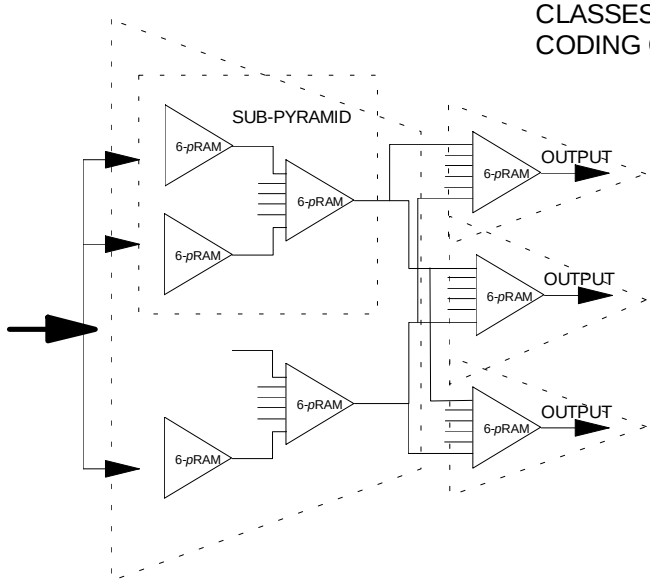
TRAINING

A REWARD MIGHT BE GIVEN TO ALL *p*RAMS IN A PYRAMID WHEN THE OUTPUT OF THAT PYRAMID IS CORRECT; A PENALTY COULD BE GIVEN OTHERWISE.

THE REWARD OR PENALTY INPUTS CAN BE GENERATED PROBABILISTICALLY TO INDICATE A REWARD OR PENALTY IN THE RANGE 0 TO 1.

AN ALTERNATIVE STRUCTURE TO FULL PYRAMIDS IS SHOWN WHICH REQUIRES FEWER *p*RAMS.

THE *N* OUTPUT PYRAMIDS INDICATE THE CLASS OF THE INPUT AND EITHER UNARY (*N* CLASSES) OR BINARY (*2^N* CLASSES) CODING CAN BE USED.



TRAINING

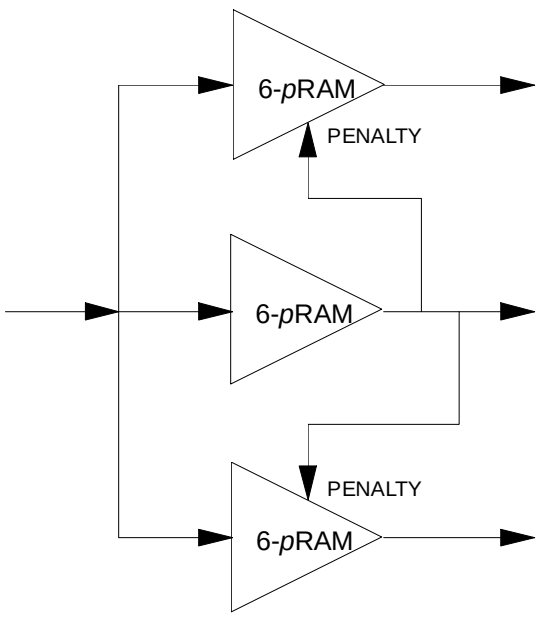
THE INPUT PYRAMIDAL LAYER(S) WOULD NORMALLY BE TRAINED FIRST AND ACT AS FEATURE DETECTORS.

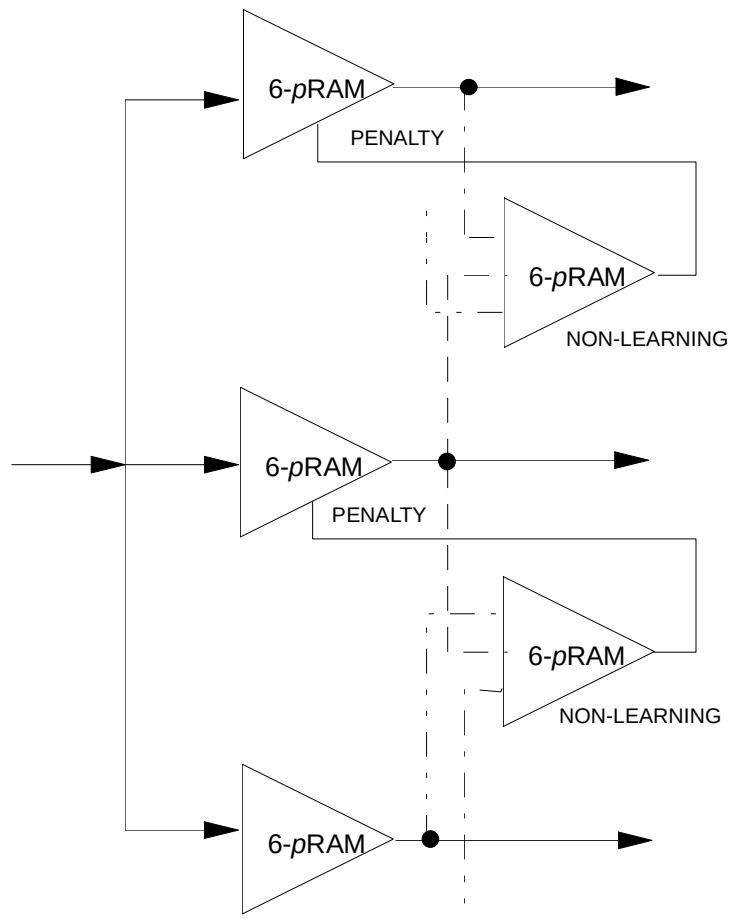
THE OUTPUT PYRAMIDS ARE TRAINED SEPARATELY AS FULL DISCRIMINATORS (UNARY CODING) OR AS A SET (BINARY CODING). THE ERROR FUNCTION IS CALCULATED ACCORDING TO THE OUTPUT CODING SELECTED AND FROM THIS, THE REWARD AND PENALTY SIGNALS ARE CALCULATED BY EXTERNAL CIRCUITS.

OTHER ARCHITECTURES

COMPETITIVE LEARNING

THE OUTPUT OF ONE *p*RAM MAY BE USED AS A PENALTY INPUT TO ANOTHER *p*RAM. IN THIS WAY, COMPETITION BETWEEN NEURONS OR MUTUAL INHIBITION CAN BE ACHIEVED. SIMILAR MECHANISMS FOR THE REWARD INPUTS CAN BE CONSTRUCTED.





A NEIGHBOURHOOD OF *p*RAMS CAN GENERATE COMPLEX PENALTY INPUTS TO ADJOINING *p*RAMS THROUGH THE USE OF NON-LEARNING *p*RAMS WHICH ALLOW THE PENALTY INPUT TO BE A NON-LINEAR FUNCTION OF THE NEIGHBOURING *p*RAM OUTPUTS.

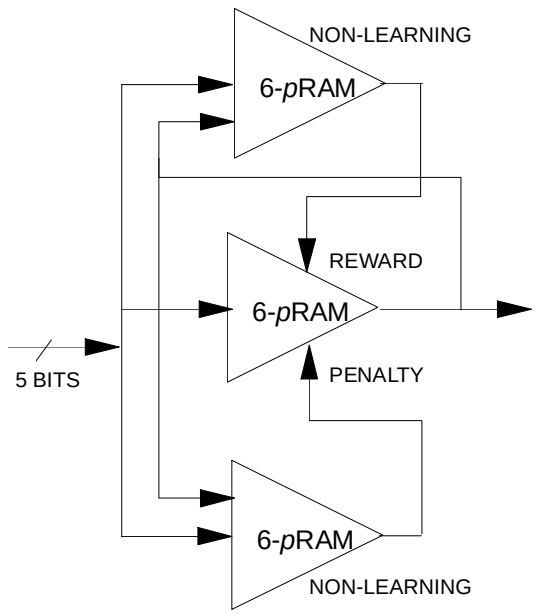
A SIMILAR ARRANGEMENT CAN BE MADE FOR THE REWARD INPUTS. THE NON-LEARNING *p*RAMS ACT AS LOOK-UP TABLES.

LOCAL LEARNING

THE NON-LEARNING (AUXILIARY) *p*RAMS DEFINE THE ACTIONS OF THE CENTRAL (LEARNING) *p*RAM WHICH ARE TO BE REWARDED OR PENALISED.

THE AUXILIARY *p*RAMS RECEIVE BOTH THE INPUT VECTOR AND THE OUTPUT OF THE LEARNING *p*RAM SO THAT ALL POSSIBLE STATES CAN BE DEFINED.

SINCE THE AUXILIARY *p*RAMS HAVE A PROBABILISTIC OUTPUT, COMPLEX REWARD/PENALTY ACTIONS CAN BE MADE.



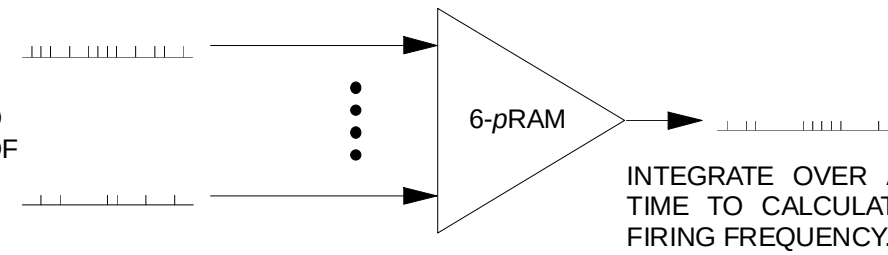
USING NON-BINARY INPUTS WITH *p*RAM NETS

A NUMBER OF SCHEMES ARE POSSIBLE TO REPRESENT NON-BINARY INPUTS TO A *p*RAM NETWORK.

a) PULSE STREAMS
b) PARALLEL BINARY INPUTS
c) UNARY INPUTS

PULSE STREAMS

REAL_VALUED INPUTS ARE CONVERTED TO SPIKE TRAINS OF A GIVEN MEAN FIRING FREQUENCY USING NON-LEARNING *p*RAMS.

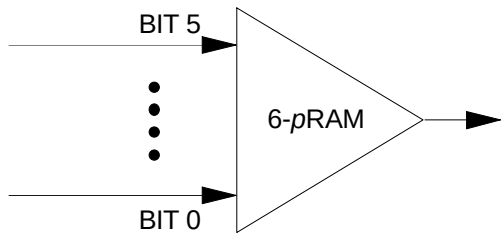


INTEGRATE OVER A PERIOD OF TIME TO CALCULATE THE MEAN FIRING FREQUENCY.

BINARY INPUTS

AN N-BIT BINARY INPUT CAN BE APPLIED IN PARALLEL TO ONE *p*RAM (IF N<=6) OR TO A NUMBER OF *p*RAMS.

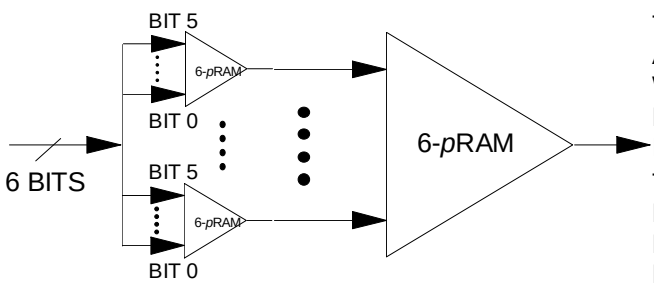
THIS METHOD IS COSTLY IN TERMS OF THE NUMBER OF *p*RAM INPUTS IT USES.



THE USE OF BINARY INPUTS DOES NOT CONVEY TO A *p*RAM NETWORK THE RELATIVE SIGNIFICANCE OF THE INDIVIDUAL BITS IN THE INPUT. THE NETWORK HAS TO LEARN THIS SIGNIFICANCE DURING TRAINING.

BINARY INPUTS

AN N-BIT BINARY INPUT CAN BE CONVERTED TO A 6-BIT UNARY CODED INPUT AS SHOWN.



THE NON-LEARNING *p*RAMS ABOVE HAVE IDENTICAL, LINEARLY-INCREASING WEIGHTS. THESE PRODUCE SIX STOCHASTIC, UNARY-CODED PULSE TRAINS FOR THE MAIN *p*RAM.

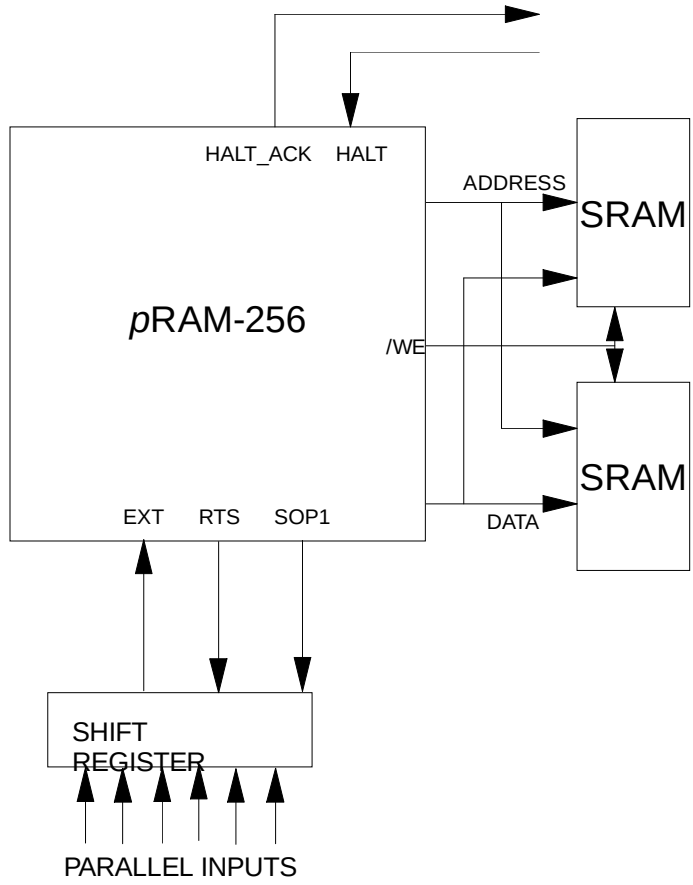
THE INPUTS TO THE *p*RAM ARE A SET OF PULSES WHOSE DENSITY IS PROPORTIONAL TO THE INPUT BINARY NUMBER.

THEREFORE THE MEMORY LOCATIONS ACCESSED ARE RELATED TO THE MAGNITUDE OF THE INPUT.

A CLUSTER OF MEMORY LOCATIONS ARE ACCESSED OVER TIME, DUE TO THE STOCHASTIC SPIKE TRAINS.

DATA INPUT TO A *p*RAM NET

TWO METHODS ARE DESCRIBED BELOW:
a) SERIAL/PARALLEL INPUT OF BINARY DATA
b) INPUT OF REAL-VALUED DATA



INPUT OF BINARY DATA

WHERE BINARY DATA IS AVAILABLE IN SERIAL FORM, THIS MAY BE ENTERED DIRECTLY INTO THE *p*RAM-256 USING THE **EXT** (EXTERNAL INPUT) PIN. THE **NORTH**, **SOUTH**, **EAST** AND **WEST** PINS MAY ALSO BE USED FOR DATA INPUT IF THESE ARE NOT USED FOR COMMUNICATIONS BETWEEN *p*RAM-256 MODULES.

SERIAL DATA IS ENTERED IN A FRAME OF 256 BITS, CLOCKED BY **RTS**. **SOP1** PROVIDES FRAME SYNCHRONISATION. SERIAL DATA IS STORED IN THE *OUTPUT LIST* WITHIN THE *p*RAM-256 AND MAY BE 'CONNECTED' TO ANY *p*RAM INPUT BY THE USE OF THE CONNECTION POINTER TABLE.

SERIAL DATA IS CONTINUOUSLY READ AT A MAXIMUM RATE OF 6000 FRAMES PER SECOND (TRAINING DISABLED) OR A RATE OF 4000 FRAMES PER SECOND (TRAINING ENABLED).

WHERE BINARY DATA IS AVAILABLE IN PARALLEL FORM, AN EXTERNAL PARALLEL TO SERIAL CONVERSION IS REQUIRED. THIS CAN BE ACHIEVED THROUGH THE USE OF A SHIFT REGISTER AS SHOWN ABOVE. THE **SOP1** STROBE CAN BE USED TO TRANSFER DATA FROM THE PARALLEL PORT TO THE SHIFT REGISTER.

INPUT OF REAL-VALUED DATA

REAL-VALUED DATA MAY BE REPRESENTED AS A SPIKE-TRAIN, WHOSE MEAN FIRING FREQUENCY IS PROPORTIONAL TO THE VALUE IT REPRESENTS.

SUCH DATA MAY BE INPUT USING THE SERIAL PORTS AS ABOVE, BUT CONVERSION OF THE DATA INTO SPIKE TRAINS MUST BE PERFORMED USING EXTERNAL HARDWARE.

ALTERNATIVELY, THE REAL-VALUED DATA MAY BE STORED, ONE VALUE PER *p*RAM, IN THE *p*RAMS' WEIGHT MEMORY. THE *p*RAMS USED IN THIS WAY ARE NON-LEARNING AND ARE ONLY USED TO GENERATE SPIKE TRAINS FOR THE INPUT LAYER OF THE NEURAL NETWORK.

IN ORDER TO WRITE TO THE SRAM WEIGHT MEMORY, THE *p*RAM-256 IS HALTED. WHEN **HALT_ACK** IS ASSERTED AT THE END OF THE PASS, THE *pRAM-*256 **ADDRESS** AND **DATA** BUSES AND **/WE** ARE TRI-STATED SO THAT THE SRAM CAN BE WRITTEN TO BY AN EXTERNAL CONTROLLER.